

FuturePlus Systems

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Advancing Technology Development



DisplayPort Protocol Analyzer for eDP 2.0 128b/132b

FS4523 and FS4524

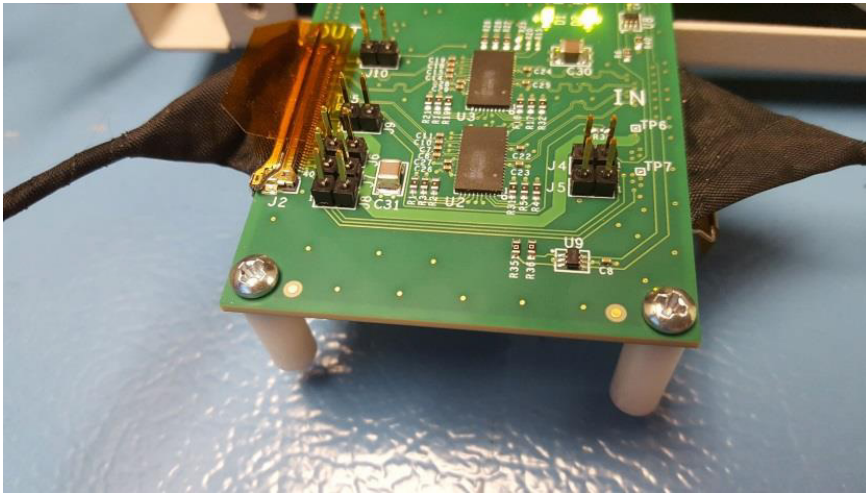


Example 40 Pin eDP Laptop Motherboard

Use YOUR Source and YOUR Sink for the ultimate in debug!



DATASHEET



Example 40 Pin eDP Probe Board

The ONLY tool on the market that **does not rely on a reference sink or source** and **monitors and triggers BOTH the high speed main link and the Aux channel!**

Complete packet by packet decode of the eDP High Speed Main Link and Aux

Multiple eDP Probe Boards available

Decodes and time correlates Aux and High Speed main link traffic

1 Gig state Main Link trace buffer allows for multiple frame capture and pixel by pixel analysis

NEW! Trigger on Settings or Decode from bits INSIDE a Packet

Key eDP 2.0 Features

- ✓ **Supports link rates up to 13.5 Gbps/lane (UHBR13.5) with full 128b/132b symbol decode and timing analysis.**
- ✓ **Backward-compatible with eDP 1.3 – 1.5 (8b/10b up to HBR3 8.1 Gbps/lane).** Real-time capture and decode of new eDP 2.0 training sequences, link-rate negotiation, and symbol transitions.
- ✓ **Comprehensive ALPM (Advanced Link Power Management) visibility,** including both AUX-wake and new AUX-less LFPS signaling, enabling full analysis of link sleep, standby, and rapid-wake behavior.
- ✓ **Full Panel Self Refresh (PSR2) and Panel Replay (PR) decode** with selective-update tracking and CRC validation.
- ✓ Integrated DSC 1.2a and FEC packet decoding to verify compressed-stream integrity at UHBR speeds.
- ✓ Correlated Main-Link and AUX analysis, showing DPCD register activity alongside video and timing events.
- ✓ Advanced trigger and filter controls for link training, power transitions, and refresh-state changes.

The FuturePlus® FS4500 DisplayPort Analysis Probe provides a mechanical, electrical and software interface to the DisplayPort, a digital display interface standard supported by the Video Electronics Standards Association (VESA).

The FS4500 is used to design, debug and verify compliance for computer motherboards, monitors, home theater systems, and silicon chips incorporating the eDP technology.



Helping you Design Tomorrow's Computers, Today

FuturePlus Systems is the technology leader in protocol analysis tools for the computer design industry. Our Interposers and software help you monitor and verify complex activities on your advanced technology computer bus design. FuturePlus systems offerings include bus-analysis solutions for most popular computer buses. Visit www.futureplus.com for more information.

Filtering Made Easy - Save Only the Events of Interest in the 16GB Trace Buffer with Hardware and Software Selective Storage Qualification

Hardware Level Selective Store Criteria – Selected Prior to Data Collection

Post-Processing Filtering applied to collected data from the Listing Screen

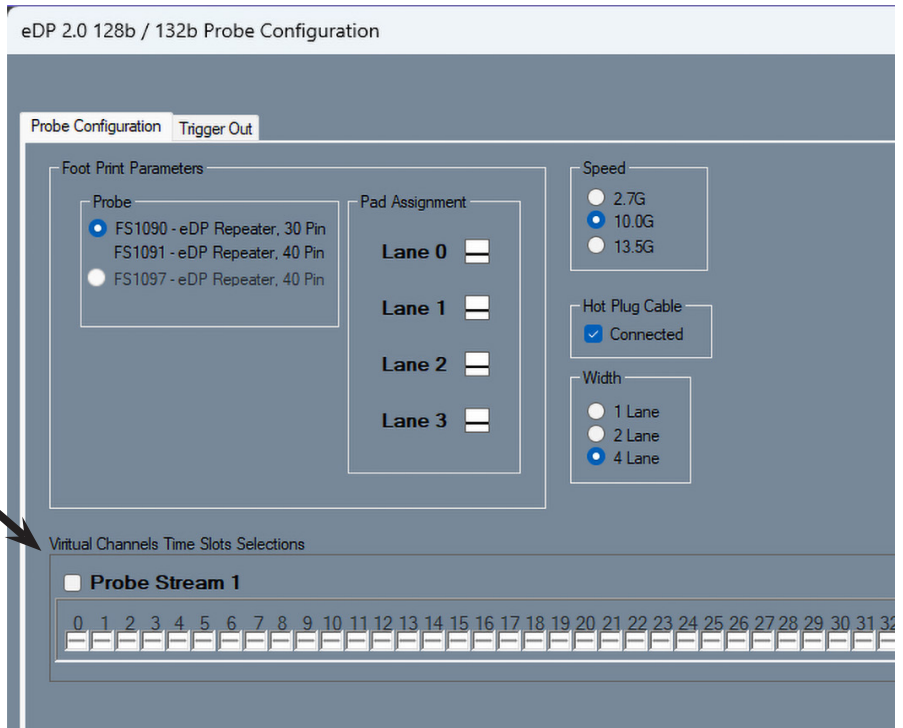
See eDP Details Down to the Exact Pixel

Marker	Sample Number	Decode	Time	Trigger	VCTag	EventCode	Ln0_Symbol_Data	Ln1_Symbol_Data	Ln2_Symbol_Data	Ln3_Symbol_Data
	-946	P756 R = 0 G = 255 B = 0 P757 R = 0 G = 255 B = 0 P758 R = 0 G = 255 B = 0 P759 R = 0 G = 255 B = 0	-36.909 μS	0	1	Hor. Pixel	FF0000FF	FF0000FF	FF0000FF	FF0000FF
	-945	P760 R = 0 G = 255 B = 0 P761 R = 0 G = 255 B = 0 P762 R = 0 G = 255 B = 0 P763 R = 0 G = 255 B = 0 P764 R = 0 G = 255 B = 0 P765 R = 0 G = 255 B = 0 P766 R = 0 G = 255 B = 0 P767 R = 0 G = 255 B = 0	-36.906 μS	0	1	Hor. Pixel	00FF0000	00FF0000	00FF0000	00FF0000
	-944	P768 R = 0 G = 255 B = 0 P769 R = 0 G = 255 B = 0 P770 R = 0 G = 255 B = 0 P771 R = 0 G = 255 B = 0	-36.899 μS	0	1	Hor. Pixel	0000FF00	0000FF00	0000FF00	0000FF00
	-943	P772 R = 0 G = 255 B = 0 P773 R = 0 G = 255 B = 0 P774 R = 0 G = 255 B = 0 P775 R = 0 G = 255 B = 0	-36.896 μS	0	1	Hor. Pixel	FF0000FF	FF0000FF	FF0000FF	FF0000FF
	-942	P776 R = 0 G = 255 B = 0 P777 R = 0 G = 255 B = 0 P778 R = 0 G = 255 B = 0 P779 R = 0 G = 255 B = 0 P780 R = 0 G = 255 B = 0 P781 R = 0 G = 255 B = 0 P782 R = 0 G = 255 B = 0 P783 R = 0 G = 255 B = 0	-36.893 μS	0	1	Hor. Pixel	00FF0000	00FF0000	00FF0000	00FF0000
	-941	P784 R = 0 G = 255 B = 0 P785 R = 0 G = 255 B = 0 P786 R = 0 G = 255 B = 0 P787 R = 0 G = 255 B = 0	-36.890 μS	0	1	Hor. Pixel	0000FF00	0000FF00	0000FF00	0000FF00
	-940	P788 R = 0 G = 255 B = 0 P789 R = 0 G = 255 B = 0 P790 R = 0 G = 255 B = 0 P791 R = 0 G = 255 B = 0	-36.698 μS	0	1	Hor. Pixel	FF0000FF	FF0000FF	FF0000FF	FF0000FF
	-939	P792 R = 0 G = 255 B = 0 P793 R = 0 G = 255 B = 0 P794 R = 0 G = 255 B = 0 P795 R = 0 G = 255 B = 0 P796 R = 0 G = 255 B = 0 P797 R = 0 G = 255 B = 0 P798 R = 0 G = 255 B = 0 P799 R = 0 G = 255 B = 0	-36.694 μS	0	1	Hor. Pixel	00FF0000	00FF0000	00FF0000	00FF0000
	-938	P800 R = 0 G = 255 B = 0 P801 R = 0 G = 255 B = 0 P802 R = 0 G = 255 B = 0 P803 R = 0 G = 255 B = 0	-36.691 μS	0	1	Hor. Pixel	0000FF00	0000FF00	0000FF00	0000FF00
	-937	P804 R = 0 G = 255 B = 0 P805 R = 0 G = 255 B = 0 P806 R = 0 G = 255 B = 0 P807 R = 0 G = 255 B = 0	-36.688 μS	0	1	Hor. Pixel	FF0000FF	FF0000FF	FF0000FF	FF0000FF

Probe Configuration - eDP High Speed Main Link Analysis

VC (Virtual Channel) Payload Time slots

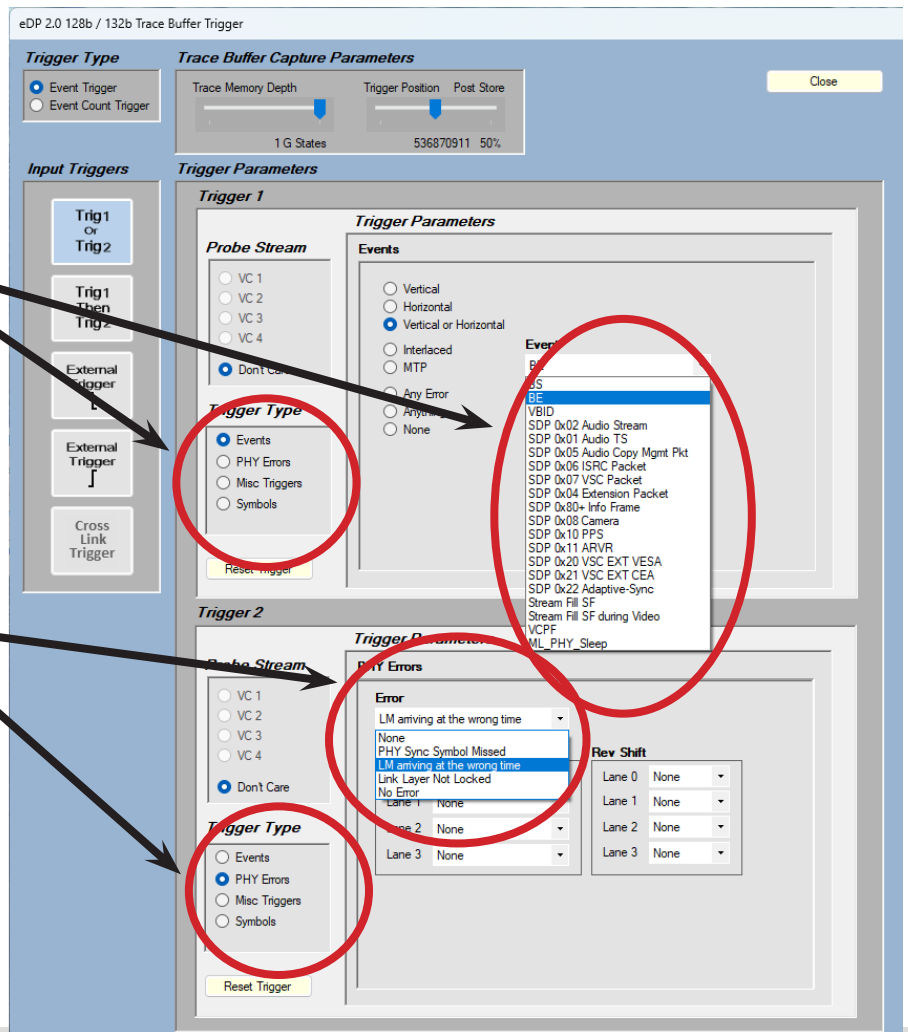
In MST mode only, the spec allows for video display information to be broken up into 64 Payload Time Slots that are assigned to the individual video streams (VCs) that are being carried on the DP link. This dialog allows the user to assign each possible Time Slot to any of the up to 4 video streams that the FS4500 probe will capture and decode.



Triggering on the Exact eDP DisplayPort Event

Trigger on Any Event

Trigger on Any PHY Error

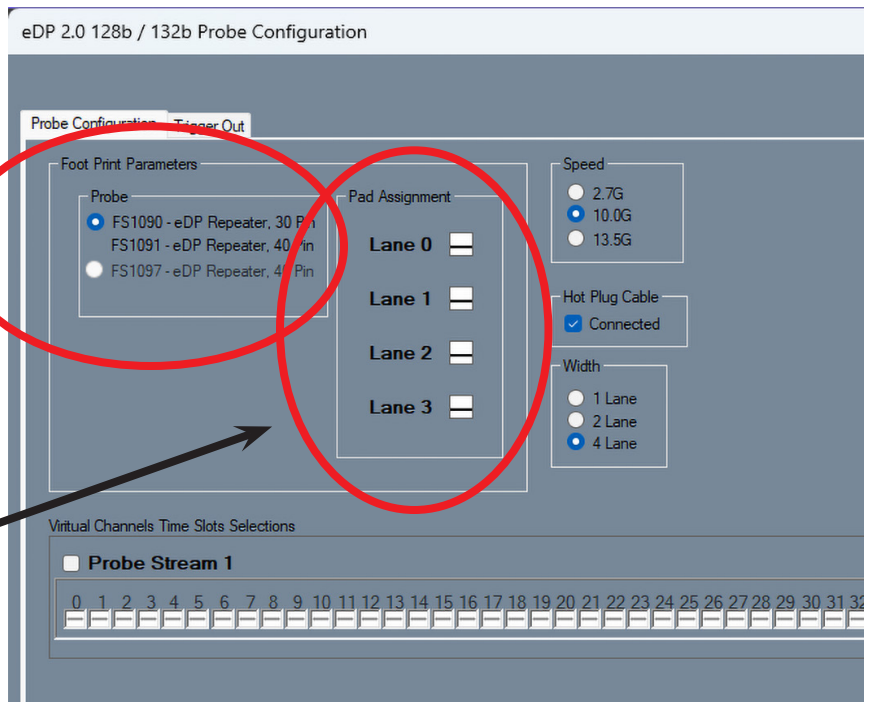


Probe Configuration - eDP High Speed Main Link Analysis

Select your Probe Board - Custom configurations are available

These buttons mirror the LEDs on the front of the FS4500.

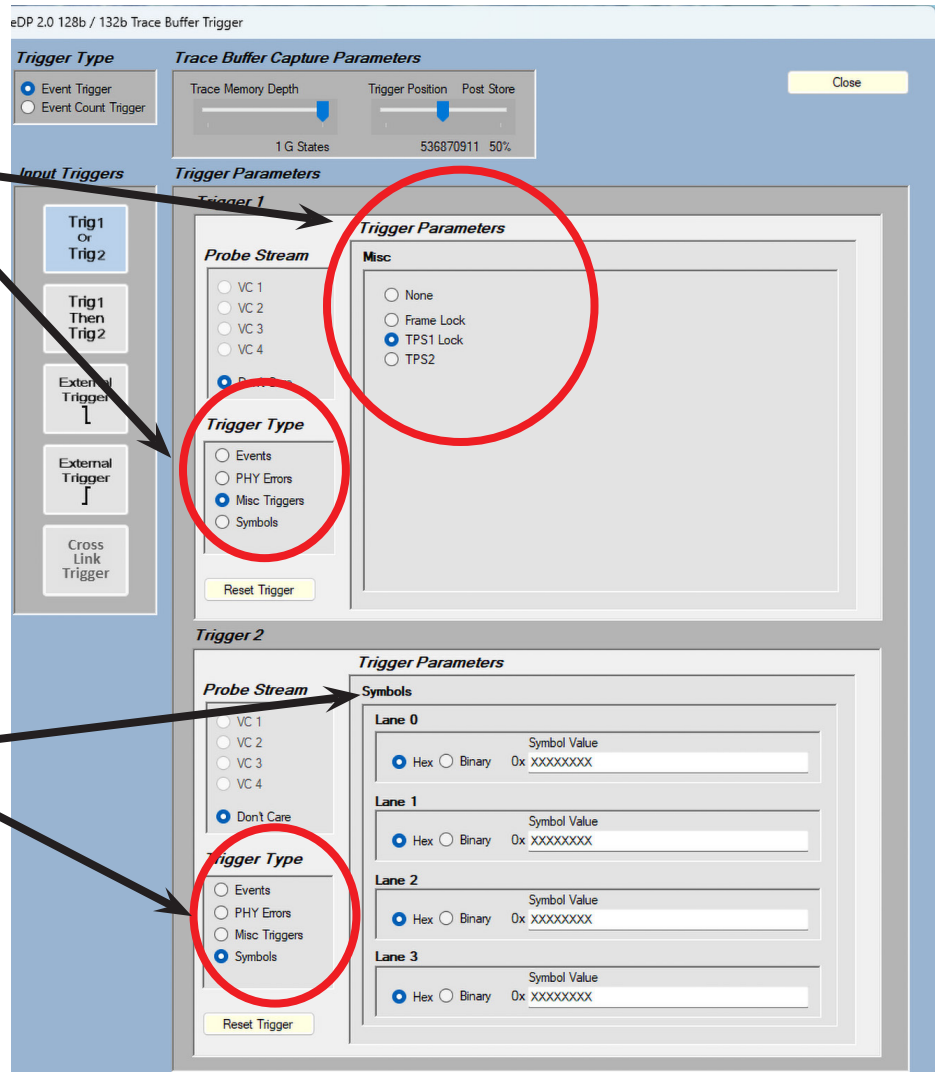
- Green - Communicating
- Red - Rx Error
- Orange - Data invalid



Advanced Triggering Options

Trigger on These Parameters

Trigger on Any Symbol



Main Stream Attribute Packet Example

eDP 2.0 128b / 132b Trace Buffer Trigger

Trigger Type

Event Trigger
 Event Count Trigger

Trace Buffer Capture Parameters

Trace Memory Depth: 4K States
Trigger Position: "2047 50"
Post Store: "2047 50"

Input Triggers

Trig1 or Trig2
Trig1 Then Trig2
External Trigger
External Trigger
Cross Link Trigger

Trigger Parameters

Trigger 1

Probe Stream

VC 1
 VC 2
 VC 3
 VC 4
 Don't Care

Events

Vertical
 Horizontal
 Vertical or Horizontal
 Interlaced
 MTP
 Any Error
 Anything
 None

Event

MSA
SDP State Offset: 0x03

Trigger Type

Events
 PHY Errors
 Misc Triggers
 Symbols

Reset Trigger

Trigger 2

Probe Stream

VC 1
 VC 2
 VC 3
 VC 4
 Don't Care

Events

Vertical
 Horizontal
 Vertical or Horizontal
 Interlaced
 MTP
 Any Error
 Anything
 None

Event

None
SDP State Offset: 0xxx

Reset Trigger

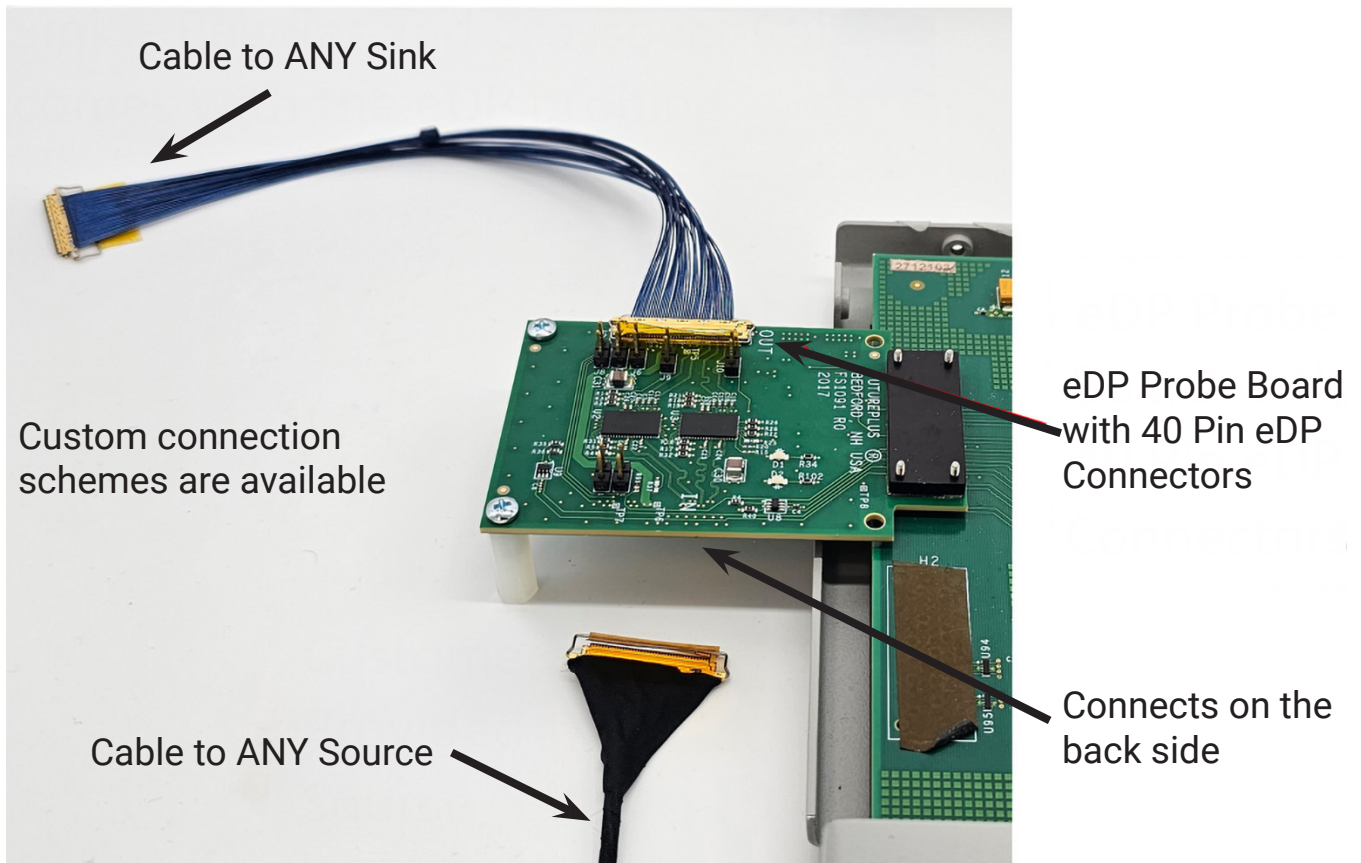
eDP 2.0 128b / 132b Main Link State Listing

File Listing Summary Validation

Marker	Sample Number	Decode	Time	Trigger	VC Tag	EventCode	Ln0_Symbol_Data	Ln1
	7	Pixel State	-211.200 nS	0	1	Hor. Pixel	00000000	0000
	4	Stream Fill SF	-208.000 nS	0	1	Hor. Stream Fill SF during Video	78377887	7837
	5	Pixel State	-204.800 nS	0	1	Hor. Pixel	00000000	0000
	4	BS	-201.600 nS	0	1	Ver. BS	D022D022	D022
	-3	VB-ID = 0x01 VerticalBlanking_Flag = 1 FieldID_Flag = 0 Interface_Flag = 0 NoVideoStream_Flag = 0 AudioMute_Flag = 0 HDCP Sync Detect = 0 CompressedStream_Flag = 0	-198.400 nS	0	1	Ver. VBID	00000001	0000
	-2	MSA SS	-6.400 nS	0	1	MSA	99669966	9966
	-1	MSA SS	-3.200 nS	0	1	MSA	F906F906	F906
T1	0	VFREQ[7.40] = 0x00000000 VFREQ[8.20] = 0x00000001 VFREQ[31.24] = 0x00000008 VFREQ[23.16] = 0x000000D9	0.000 nS	1	1	MSA	08000000	0000
	1	Hor. Total(Pixels) = 2200 Hor. Start(Pixel) = 192 Hor. Width(Pixels) = 1920 VFREQ[15.8] = 0x000000EE VFREQ[7.0] = 0x00000020 Ver. Total(Line Count) = 1125 Ver. Start(Line Count) = 41 Ver. Height = 1080 MISC0 = 32 Link & Stream Clks: Asynchronous Colorimetry = Legacy RGB ColorDepth = 8 Bits/color MISC1 = 0 # Of Interlaced Lines: Is Odd # Stereo Video Atr: No Stereo Video	3.200 nS	0	1	MSA	00650498	0029
	2	Hor. Sync Polarity: Active High Pulse Hor. Sync Width(Pixels) = 44 Ver. Sync Polarity: Active High Pulse Ver. Sync Width(Pixels) = 5	6.400 nS	0	1	MSA	0000002C	0000
	3	MSA SE	9.600 nS	0	1	MSA	B445B445	B445
	4	VC PF	204.800 nS	0	1	Ver. VCPF	96659663	9663
	5	Secondary Pkt Start	208.000 nS	0	1	Ver. Audio Stream	F906F906	F906
	6	HB0 Pkt ID: 0 HB1 Pkt Type[2]: Audio Stream HB2 16 Channel Layout 64k sample freq HB3 Channel Count: Stereo01 2 to 8 channel LPCM 192khz content/IEC 61937 encoded content with Bt rate <= 5.144Mbps	211.200 nS	0	1	Ver. Audio Stream	00000000	0000
	7	S0_C0.0x00000000 S1_C0.0x00000000 S2_C0.0x00000000 S3_C0.0x00000000	214.400 nS	0	1	Ver. Audio Stream	00009000	0000
	8	Secondary Pkt End	217.600 nS	0	1	Ver. Audio Stream	1AE51AE5	1AE5
	9	Stream Fill SF	220.800 nS	0	1	Ver. Stream Fill SF	F807F807	F807

eDP 128b/132b Trace Buffer Trigger

eDP 128b/132b Main Link State Listing



40 Pin eDP VESA Standard Probe Board shown above

Trigger on Aux Command and/or Address to Find Events Quickly - And Capture Main Link Traffic too!

Trigger on Aux Phy_Wake

Trigger on ANY Aux Command and store Aux AND Main Link Traffic

eDP 2.0 Aux Channel Link State Listing

File Listing Summary

Marker	Sample Number	Decode	Aux_Time	Aux_Trig_Stat	Time	PHY_Wake	Data	Address	Command
	3541	DOWN REQ	00:00:01.3995680	0	-00:00:03.1462200	0	10	1000	Aux Write
	3542	DOWN REQ	00:00:01.3995760	0	-00:00:03.1462200	0	46	1000	Aux Write
	3543	DOWN REQ	00:00:01.3995840	0	-00:00:03.1462200	0	C5	1000	Aux Write
	3544	DOWN REQ	00:00:01.3995919	0	-00:00:03.1462200	0	11	1000	Aux Write
	3545	DOWN REQ	00:00:01.3996000	0	-00:00:03.1462200	0	90	1000	Aux Write
	3546	DOWN REQ	00:00:01.3996080	0	-00:00:03.1462200	0	2	1000	Aux Write
	3547	DOWN REQ	00:00:01.3996160	0	-00:00:03.1462200	0	2	1000	Aux Write
	3548	DOWN REQ	00:00:01.3996239	0	-00:00:03.1462200	0	15	1000	Aux Write
	3549	DOWN REQ	00:00:01.3996320	0	-00:00:03.1462200	0	1C	1000	Aux Write
	3550	Aux ACK All Data bytes written	00:00:01.3997539	0	-00:00:03.1462200	0	0	0	Ack
	3551	Aux Read request, Address = 200 Length = 6	00:00:01.4038880	0	-00:00:03.1462200	0	5	200	Aux Read
	3552	Aux ACK Sink Count = 1 CP ready = 1	00:00:01.4040700	0	-00:00:03.1462200	0	41	0	Ack
	3553	DEVICE_SERVICE_IRQ_VECTOR Remote Control Cmd pending = 0 CP IRQ = 0 MCCC IRQ = 0 Down Rep MSG Ready = 1 Up Req MSG Ready = 0 Sink Specific IRQ = 0	00:00:01.4040779	0	-00:00:03.1462200	0	10	0	Ack
	3554	LANE 0 AND 1 STATUS Lane0 CR Done = 1 Lane0Channel EQ Done = 1 Lane0Symbol locked = 1 Lane1CR Done = 1 Lane1Channel EQ Done = 1 Lane1Symbol locked = 1	00:00:01.4040860	0	-00:00:03.1462200	0	77	0	Ack
	3555	LANE 2 AND 3 STATUS Lane2 CR Done = 1 Lane2Channel EQ Done = 1 Lane2Symbol locked = 1 Lane3CR Done = 1 Lane3Channel EQ Done = 1 Lane3Symbol locked = 1	00:00:01.4040939	0	-00:00:03.1462200	0	77	0	Ack
	3556	LANE ALIGN STATUS UPDATED Interlane_align done = 1 Downstream port status changed = 0 Link status updated = 0	00:00:01.4041020	0	-00:00:03.1462200	0	D	0	Ack
	3557	SINK STATUS Receive Port 0 status = Sink out of sync Receive Port 1 status = Sink in sync Stream Regeneration Status = Stream is not being regenerated Interhop AUX Reply Indication = 0	00:00:01.4041099	0	-00:00:03.1462200	0	2	0	Ack
	3558	Aux Read request, Address = 2007 Length = 1	00:00:01.4041959	0	-00:00:03.1462200	0	0	2007	Aux Read
	3559	Aux ACK SU_PSR_EVENT_STATUS_INDICATOR SINK DEVICE SU_PSR CAPABILITY CHANGE = No PSR1/PSR2 capability	00:00:01.4042819	0	-00:00:03.1462200	0	0	0	Ack
	3560	Aux Read request, Address = 1400 Length = 16	00:00:01.4045539	0	-00:00:03.1462200	0	F	1400	Aux Read
	3561	Aux ACK DOWN REP	00:00:01.4046580	0	-00:00:03.1462200	0	10	0	Ack
	3562	DOWN REP	00:00:01.4046659	0	-00:00:03.1462200	0	46	0	Ack
	3563	DOWN REP	00:00:01.4046740	0	-00:00:03.1462200	0	C5	0	Ack

Aux Channel Traffic is Presented in an Easy to Read Format

Time Correlated to the High-Speed Main Link so Cause and Effect can be Quickly Analyzed

Aux Channel State Summary

eDP 2.0 Aux Channel Link State Listing

File Listing Summary

Listing 1 Summary

- Receiver Capability: 0x0 - 0xFF
- Link Configuration: 0x100 - 0x1FF
- Link/Sink Device Status: 0x200 - 0x2FF
- Source Device-specific: 0x300 - 0x3FF
- Sink Device-specific: 0x400 - 0x4FF
- Branch Device-specific: 0x500 - 0x5FF
- Link/Sink Device Power Control: 0x600 - 0x6FF
- eDP-specific: 0x700 - 0x7FF
- RESERVED: 0x800 - 0xFFF
- Sideband MSG Buffers: 0x1000 - 0x17FF
- RESERVED: 0x1800 - 0x1FFF
- DPRX Event Status Indicator: 0x2000 - 0x21FF
- Extended Receiver Capability: 0x2200 - 0x22FF
- RESERVED: 0x2300 - 0x2FFF
- ProtoCol Converter Extension: 0x3000 - 0x30FF
- RESERVED: 0x3100 - 0x5FFFF
- Multi-touch: 0x60000 - 0x61CFF
- RESERVED: 0x61D00 - 0x67FFF
- HDCP 1.3 and HDCP2.2: 0x68000 - 0x69FFF
- RESERVED: 0x6A000 - 0xEFFFF
- LT-tunable PHY Repeater: 0xF0000 - 0xF02FF
- RESERVED: 0xF0300 - 0xFFEFF
- MyDP-specific: 0xFFFF00 - 0xFFFFF

GetSummary

Address 0x100:
Data 0x01
LINK_BW_SET
Link BW Set = 10 Gbps/lane

Address 0x101:
Data 0x04
LANE_COUNT_SET
Lane Count Set = Four Lanes (Lane 0,1,2,and 3)
Post LT ADJ REQ Granted = Not granted
Enhanced Frame EN = Is Not Enabled

Address 0x102:
Data 0x00
TRAINING_PATTERN_SET
TRAINING_PATTERN_SELECT = Training not in progress
if DPCD 00108h == 01h bit 4 is decoded as follows:
RECOVERED_CLOCK_OUT_EN = Disabled
If DPCD 00108h == 02h, bit 4 is reserved
SCRAMBLING_DISABLE = Scrambling Disable = Scrambler enabled
SYMBOL_ERROR_COUNT_SEL = Count disparity and illegal symbol errors

Address 0x103:
Data 0x00
TRAINING_LANE0_SET
VOLTAGE_SWING_LEVEL = level 0
MAX_SWITNG_REACHED = 0
PRE_EMPHASIS_SET = 0
MAX_PRE_EMPHASIS_REACHED = 0
If DPCD == 02h bits 3:0 are decoded as:
TX_FFE_PRESET_VALUE = 0

Address 0x104:
Data 0x00
TRAINING_LANE1_SET
VOLTAGE_SWING_LEVEL = level 0
MAX_SWITNG_REACHED = 0
PRE_EMPHASIS_SET = 0
MAX_PRE_EMPHASIS_REACHED = 0
If DPCD == 02h bits 3:0 are decoded as:
TX_FFE_PRESET_VALUE = 0

Address 0x105:
Data 0x00
TRAINING_LANE2_SET
VOLTAGE_SWING_LEVEL = level 0
MAX_SWITNG_REACHED = 0
PRE_EMPHASIS_SET = 0
MAX_PRE_EMPHASIS_REACHED = 0
If DPCD == 02h bits 3:0 are decoded as:
TX_FFE_PRESET_VALUE = 0

Address 0x106:
Data 0x00

Easily access ALL of the Aux Channel
DPCD (DisplayPort Configuration Data) Registers

Excellent for Debugging!

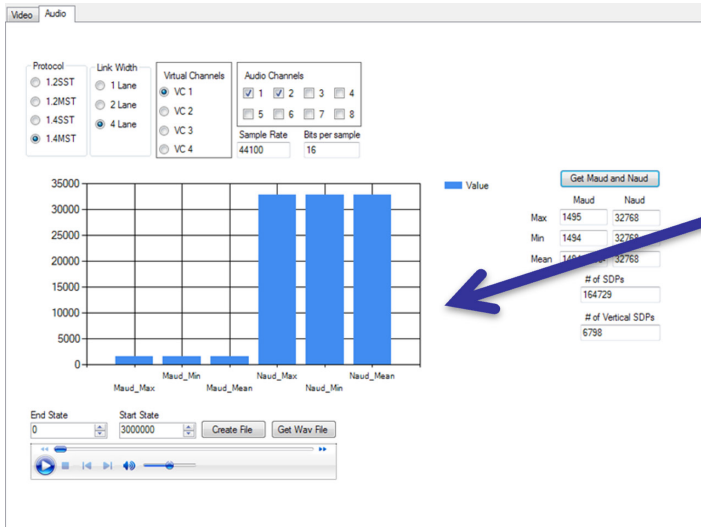
Frame Display SW

Uses the Pixels Captured by the FS4500 to Repaint the Frame

The image shows two windows from the FS4500 DisplayPort eDP Protocol Analyzer. The left window is the 'Trace Buffer Trigger' configuration screen, showing 'Trigger Type' (Event Trigger), 'Trace Buffer Capture Parameters' (4K States, 2047 50%), and 'Input Triggers' (Trig1, Trig2, External, Cross Link). The right window is the 'Main Link State Listing' showing a table of captured events.

Marker	Sample Number	Decode	Time	Trigger	VC Targ	EventCode	Ln0_Symbol_Data	Ln1
-7		Pixel State	-211.200 nS	0	1	Hor. Pixel	00000000	0000
-6		Stream Fill SF	-208.000 nS	0	1	Hor. Stream Fill SF during Video	78877887	7887
-5		Pixel State	-204.800 nS	0	1	Hor. Pixel	00000000	0000
-4		BS	-201.600 nS	0	1	Ver. BS	DD2D0D22	DD22
-3		VB-ID = 0x01 VerticalBlanking_Flag = 1 FieldID_Flag = 0 Interface_Flag = 0 NoVideoStream_Flag = 0 AudioMute_Flag = 0 HDCP Sync Detect = 0 CompressedStream_Flag = 0	-198.400 nS	0	1	Ver. VBID	00000001	0000
-2		MSA SS	-6.400 nS	0	1	MSA	99669966	9966
-1		MSA SS	-3.200 nS	0	1	MSA	F906F906	F906
T1	0	VFREQ(47.40) = 0x00000000 VFREQ(49.30) = 0x00000000 VFREQ(15.0) = 0x0000000E VFREQ(7.0) = 0x00000020 Ver. Total(Line Count) = 1125 Ver. Start(Line Count) = 41 Ver. Height = 1080 MISC0 = 32 Link & Stream Cks: Asynchronous Colorimetry = Legacy RGB ColorDepth = 8 bits/color MISC1 = 0 # Of Interlaced Lines: Is Odd # Stereo Video Attr: No Stereo Video	0.000 nS	1	1	MSA	08000000	0000
1		Hor. Total(Pixels) = 2200 Hor. Start(Pixel) = 192 Hor. Width(Pixels) = 1920 VFREQ(15.0) = 0x0000000E VFREQ(7.0) = 0x00000020 Ver. Total(Line Count) = 1125 Ver. Start(Line Count) = 41 Ver. Height = 1080 MISC0 = 32 Link & Stream Cks: Asynchronous Colorimetry = Legacy RGB ColorDepth = 8 bits/color MISC1 = 0 # Of Interlaced Lines: Is Odd # Stereo Video Attr: No Stereo Video	3.200 nS	0	1	MSA	00550498	0029
2		Hor. Sync Polarity: Active High Pulse Hor. Sync Width(Pixels) = 44 Ver. Sync Polarity: Active High Pulse Ver. Sync Width(Pixels) = 5	6.400 nS	0	1	MSA	0000002C	0000
3		MSA SE	9.600 nS	0	1	MSA	BA45BA45	BA45
4		VCPF	204.800 nS	0	1	Ver. VCPF	96699669	9669
5		Secondary Pkt Start HBD Pkt ID: 0 HB1 Pkt Type(2): Audio Stream HB2 16 Channel Layout 64k sample freq HB3 (Channel Count): Stereo01 2 to 8 channel LPCM 192kHz content/IEC S1937 encoded content with Bitrate <= 6.144Mbps	208.000 nS	0	1	Ver. Audio Stream	F906F906	F906
6		S0_CD 0x00000000 S1_CD 0x00000000 S2_CD 0x00000000 S3_CD 0x00000000	211.200 nS	0	1	Ver. Audio Stream	00000000	0000
7		S0_CD 0x00000000 S1_CD 0x00000000 S2_CD 0x00000000 S3_CD 0x00000000	214.400 nS	0	1	Ver. Audio Stream	00009000	0000
8		Secondary Pkt End	217.600 nS	0	1	Ver. Audio Stream	1A5E1A5E	1A5E

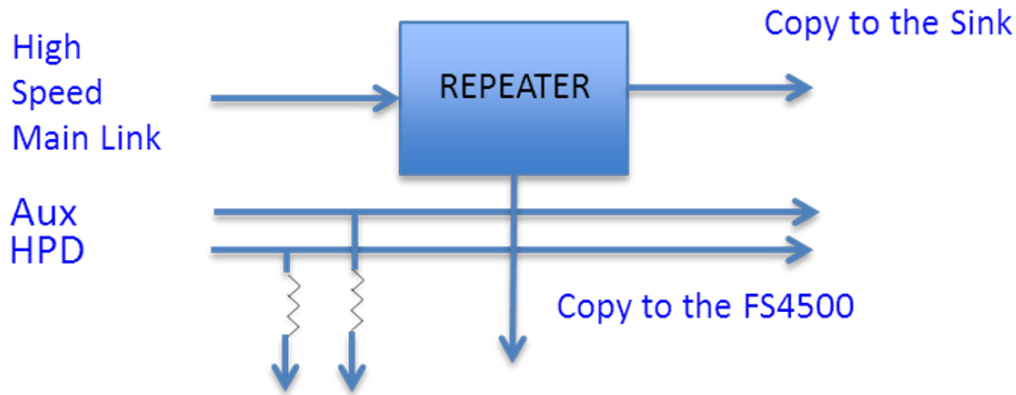
Audio Playback Software Takes the Acquired Audio Packets and Plays Them



The screenshot shows the 'Main Link State Listing' window, displaying a table of captured events. A blue arrow points from the 'Naud_Max' value in the playback software to the 'Naud' value in the table.

Marker	Sample Number	Decode	Trigger	Time	EventCode	Lane0	Lane1	Lane2	Lane3
-1		BS	0	-30.86 nS	Ver. BS	18C	18C	18C	18C
T1	0	Secondary Pkt Start	1	0 nS	Ver. Audio Stream SDP	19C	19C	19C	19C
1		HB2 Pkt ID: 0 HB1 Pkt Type(2): Audio Stream HB3 Channel Count: 01 Coding Type = 0 PB0: 00 PB1: CE PB2: 00 PB3: 67	0	6.172 nS	Ver. Audio Stream SDP	0	2	0	1
2			0	12.344 nS	Ver. Audio Stream SDP	0	CE	0	67
3			0	18.516 nS	Ver. Audio Stream SDP	0	0	0	0
4			0	24.688 nS	Ver. Audio Stream SDP	CE	D7	0	0
5			0	30.86 nS	Ver. Audio Stream SDP	CE	D7	0	0
6		S0_C1 0x00000000 S0_C2 0xA0270700 S1_C1 0x00000000 S1_C2 0x00000000	0	37.032 nS	Ver. Audio Stream SDP	90	A0	0	0
7		PB4: 39 PB5: 00 PB6: 00 PB7: 00	0	43.204 nS	Ver. Audio Stream SDP	39	82	0	0
8			0	49.376 nS	Ver. Audio Stream SDP	0	0	0	0
9			0	55.548 nS	Ver. Audio Stream SDP	0	0	0	0
10			0	61.72 nS	Ver. Audio Stream SDP	0	0	0	0
11		S0_C1 0x00000000 S0_C2 0x00000000 S1_C1 0x00000000 S1_C2 0x00000000	0	67.892 nS	Ver. Audio Stream SDP	0	0	0	0
		PB8: 90 PB9: 00							

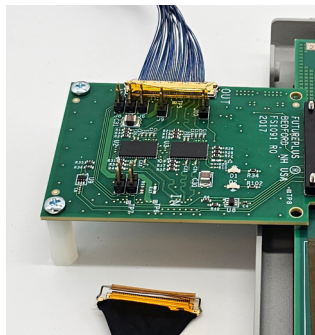
Repeater Block Diagram: Recommended Probing for eDP 1.4b and 1.5a



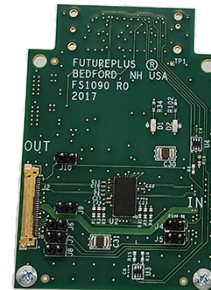
Repeater Probing

All signals are passed through with minimal skew. The output voltage follows the input within the range of 600mV to 1.3V.

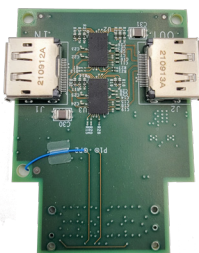
Note: The bit rate at which the probing will support is highly dependent on the target signal strength and quality.



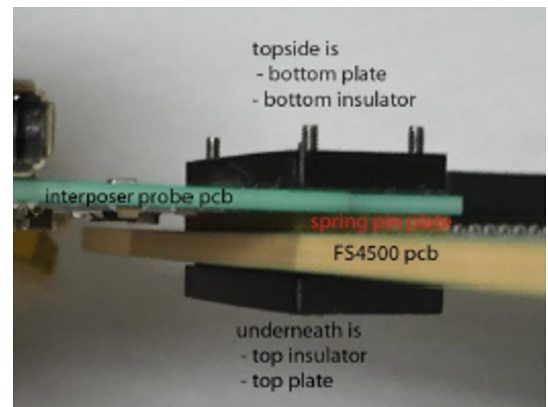
FS1091
eDP 40 Pin Repeater for the FS4500



FS1090
eDP 30 Pin Repeater for the FS4500



FS1046
DP HBR3/UHBR10 Repeater probe for FS4500 - DP
Connector also used for eDP



Ordering Information

FS4500	DisplayPort v1.2a/v1.4b and eDP1.3 Protocol Analyzer
FS4504A	Add eDP 1.4b/eDP 1.5a support FS4500
FS4506	Add 8b & 10b DSC and FEC support FS4500
FS4507	FS4500 Remote Interface for DP 1.4 and eDP
FS4509	FS4500 DP 1.4 Memory Upgrade 1G to 2G Trace
FS4520	DisplayPort CheckDPSpec Software
FS4523	eDP 2.0 128b/132b Upgrade to the FS4525
FS4524	eDP 2.0 128b/132b Upgrade to the FS4500
FS4525	DP 2.1 Upgrade for FS4500 UHBR10 and UHBR13.5 Support

eDP Probes and Adapters

FS1090	eDP 30 Pin Repeater for the FS4500
FS1091	eDP 40 Pin Repeater for the FS4500
FS1096	eDP 60 Pin Repeater for the FS4500
FS1097	eDP 40 Pin Repeater to 20 GHz
FS1200	eDP Adapters
	Custom 50 pin Source to FS1091 Cable Adapter
	FS1091 to 40 pin, .4 pitch, 20cm cable length cable adapter
	FS1091 to 40 pin, .5 pitch, 20cm cable length cable adapter
	FS1091 to 30 pin, .5 pitch, 20cm cable length cable adapter
	FS1091 to 30 pin, .5 pitch, 20cm cable length cable adapter
	FS1091 to 40 pin, .5 pitch, 20cm cable length cable adapter
	FS1091 to 40 pin, .4 pitch, 30cm cable length cable adapter
	FS1091 to 30 pin, .5 pitch, 30cm cable length cable adapter

Software included: Probe Manager, runs on a Windows based laptop or PC, supports Windows 11 and earlier.

FuturePlus Systems



Advancing Technology Development

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